NISIN

触摸显示模组产品规格承认书

Displaly Module Specifications for Approval

客户： 客户型号：			NS430QH3003AZ01		
批准 APPROVED	审核 CHECKED	拟制 DESIGNED	批准 APPROVED	审核 CHECKED	拟制 DESIGNED

修改记录

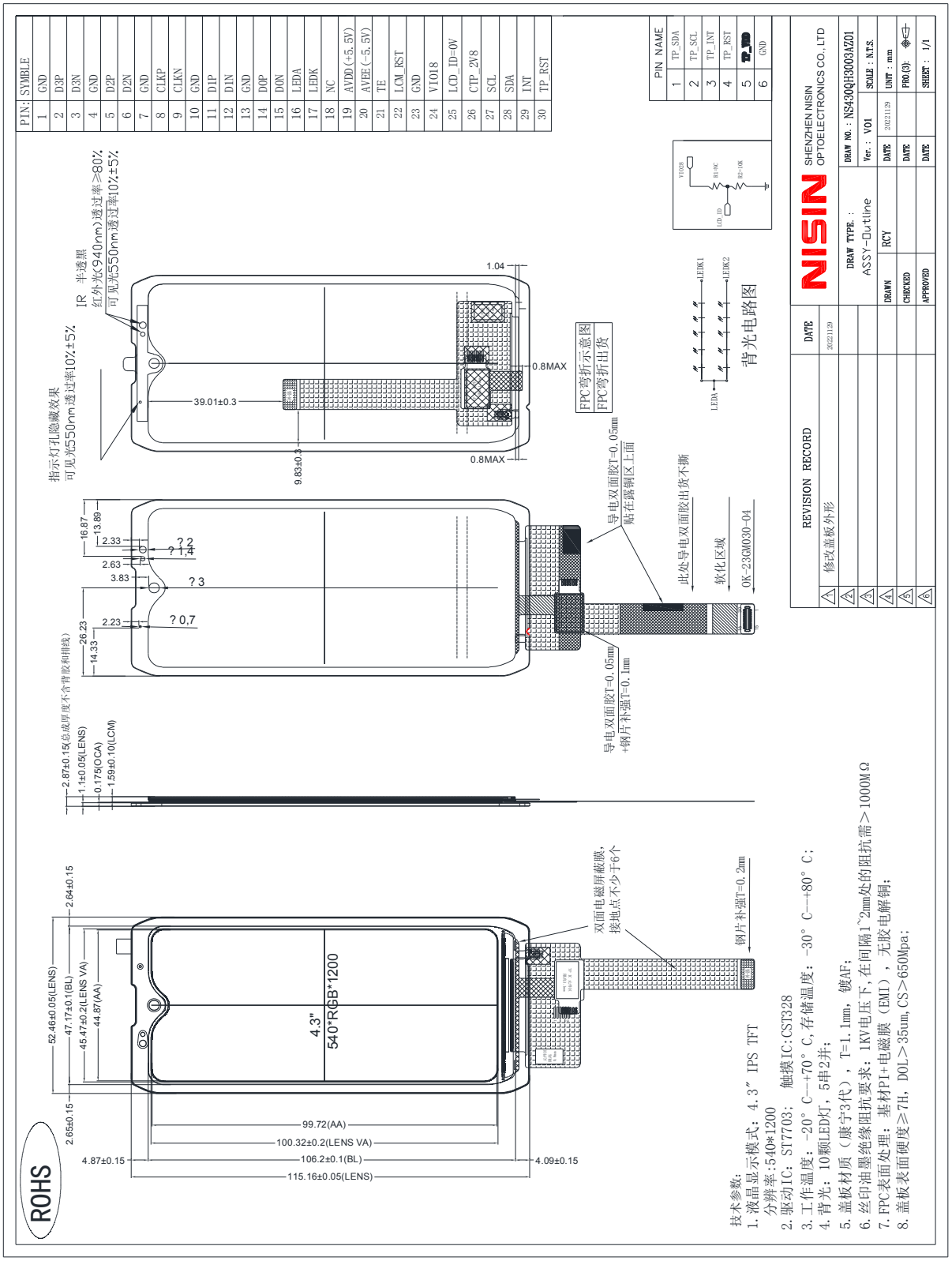
日期	版本	修改内容	页数	拟制
2022-12-06	V00	**初版发行**	所有	

目录

1.产品规格（Product Specifications）

面板类型（Panel Type）	TFT LCD
面板尺寸(Panel Size)	4.3 inch
显示类型（Display Type）	Normal Black
分辨率（Resolution）	540 (RGB) x 1200(dot)
显示点间距（Dot Pitch）	0.0281mm X 0.0843mm
显示色彩（color）	16.7M
视角（View Angle）	U/D/L/R: 80/80/80/80
显示驱动 IC（Display Driver IC）	ST7703
接口类型（Interface Type）	MIPI
触摸类型（TP Type）	I2C
触摸 IC （TP IC）	CST328
外形尺寸（Dimensions）	52.46(H) X 115.16 (V) X 2.87(T)(mm)
显示区尺寸（Display area）	44.87x 99.72(mm)
模组亮度（Module Brightness）	550cd/m²
触摸点数 Touch points	5
触摸按键 Touch Key Number	0
触摸屏固件版本	Version:

2.产品图纸（Product Drawings）



3. 接口定义（The Interface Definition）

见 CAD 图纸

4.电性特性（Electrical Characteristics）

7. Electrical Characteristics

7.1 Absolute maximum ratings

Item	Symbol	Unit	Spec.		
			Min.	Typ.	Max.
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3	-	+5.5
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3	-	+6.6
Power Supply Voltage 3	VSP ~ VSSA	V	-0.3	-	+6.6
Power Supply Voltage 4	VSSA ~ VSN	V	-0.3	-	+6.6
Power Supply Voltage 5	VGH ~ VGL	V	-0.3	-	+35
Logic Input Voltage	V_{IN}	V	-0.3	-	IOVCC+0.3
Logic Output Voltage	Vo	V	-0.3	-	IOVCC+0.3
Differential Input Voltage	DSI_CP/DSI_CN DSI_D0P/DSI_D0P, DSI_D1P/DSI_D1N	V	-0.3	-	2.0
Operating Temperature	Topr	℃	-40	-	+85
Storage Temperature	Tstg	℃	-55	-	+110

Table 7.1: Absolute Maximum Ratings

7.2 DC characteristics

7.2.1 Basic Characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Power & Operating Voltages						
Logic Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	2.0	V
Analog Operating voltage	VCI	Operation voltage	2.5	-	6.2	
Input / Output						
Logic High level input voltage	VIH	-	0.7IOVCC	-	IOVCC	V
Logic Low level input voltage	VIL	-	VSSD	-	0.3IOVCC	
Logic High level output voltage	VOH	IOH = -1.0mA	0.8IOVCC	-	IOVCC	
Logic Low level output voltage	VOL	IOL = +1.0mA	VSSD	-	0.2IOVCC	
Input leakage current	IIL	-	-1	-	1	µA
DC/DC Converter Operation						
VSP booster voltage	VSP	IVSP=1mA	4.5		6.2	V
VSN booster voltage	VSN	IVSN=-1mA	-6.2		-4.5	
VGH booster voltage	VGH	Ivgh=1mA	10		20	
VGL booster voltage	VGL	Ivgl=-1mA	-15		-7.5	
VGH and VGL difference	|VGH-VGL|	-	-	-	32	
Oscillator tolerance	OSC	25℃	-3		3	%
Source Driver						
Gamma reference voltage	VSPR	-	3.3		5.6	V
	VSNR	-	-5.6		-3.3	
Output voltage deviation	DVOS	VSSD+1.0 ~ VSPROUT-1.0	-	-	+/- 20	mV
		VSSD+0.1V ~ VSSD+1.0 VSPR-1.0 ~ VSPR-0.1V	-	-	+/- 50	mV
Output offset voltage	Voff	-		-	+/-50	mV

7.2.2 DSI DC Characteristics

LP Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX(CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX(CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX(D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX(D0)	-50	-	50	mV
Logic high level input current	V_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic low level input current	V_{IL}	LP-CD, LP-RX	-10	-	-	uA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/1	-	-	300	Vps

Figure 7.1: Input glitch rejections of low-power receivers

High Speed Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Input common mode	V_{CMCLK} V_{CMDATA}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	70	-	330	mV
Input common mode variation <450 MHZ	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-50	-	50	mV
Input common mode variation >450 MHZ	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	100	mV
Low-level differential Input threshold	V_{THLCLK} $V_{THLDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-70	-	-	mV
High-level differential Input threshold	V_{THHCLK} $V_{THHDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	70	mV
Single ended input low voltage	V_{ILHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-40	-	-	mV
Single ended input high voltage	V_{IHHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERMEN}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	450	mV
Termination capacitor	C_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	-	pF

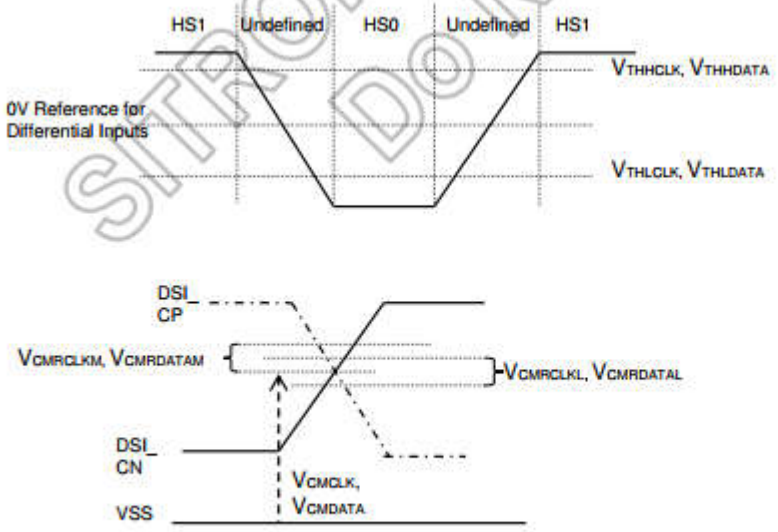


Figure 7.2: Differential voltage range and Command mode voltage

7.3.2 DSI Interface Timing Characteristics

High Speed Mode

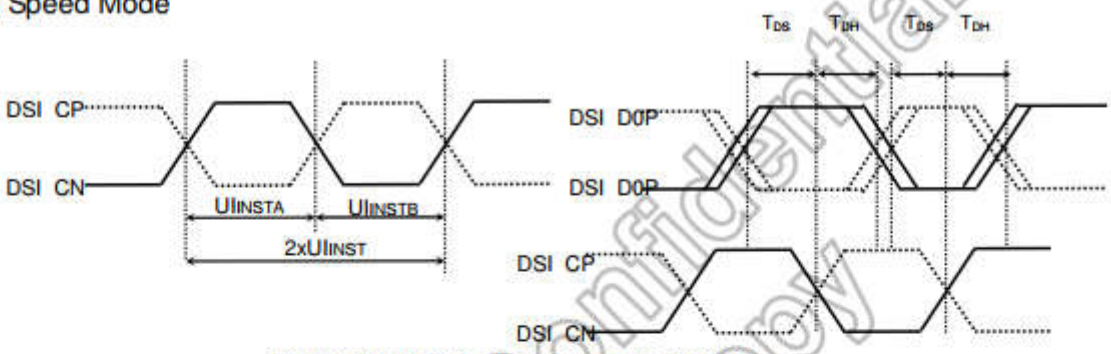


Figure 7.4: DSI clock timing Characteristics

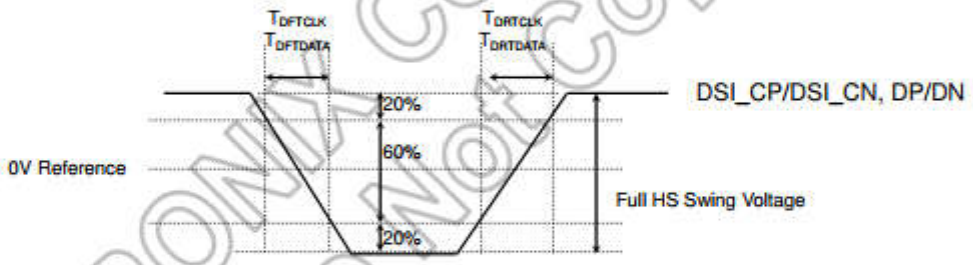


Figure 7.5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	$2xU_{INST}$	TBD	-	25	ns
	UI instantaneous	U_{INSTA} U_{INSTB}	TBD	-	12.5	ns
DP/DN	Data to clock setup time	T_{DS}	0.15xUI	-	-	ps
	Data to clock hold time	T_{DH}	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	T_{DRTCLK}	150	-	0.3UI	ps
	Differential fall time for clock	T_{DFTCLK}	150	-	0.3UI	ps
DP/DN	Differential rise time for data	$T_{DRTDATA}$	150	-	0.3UI	ps
	Differential fall time for data	$T_{DFTDATA}$	150	-	0.3UI	ps

Low Power Mode

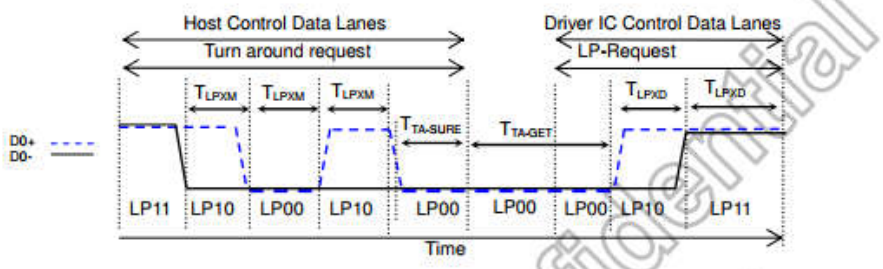


Figure 7.6: BTA from HOST to Display Module Timing

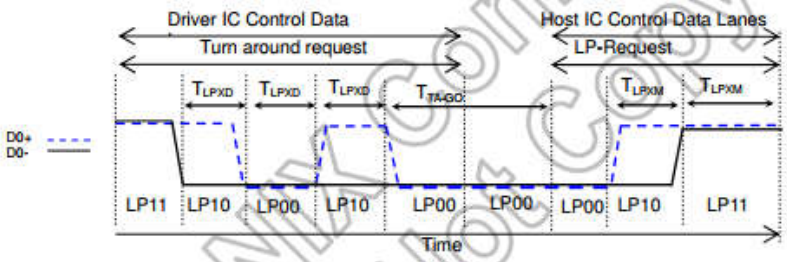


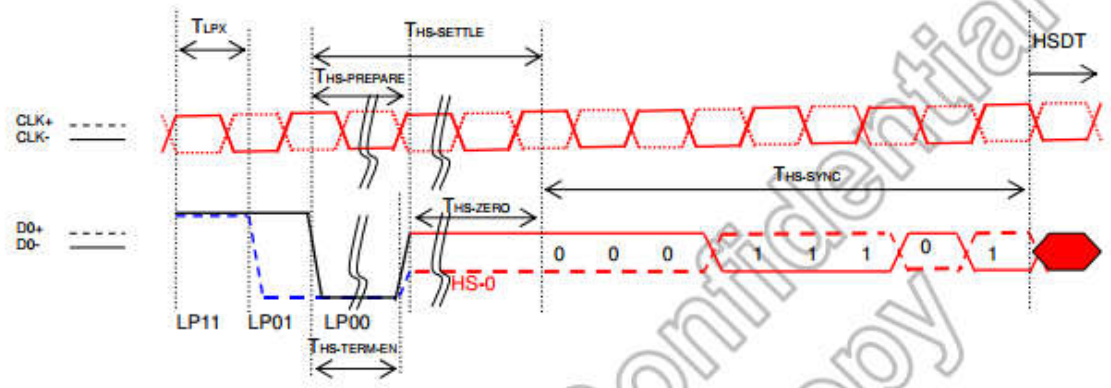
Figure 7.7: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	2xT_{LPXD}	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

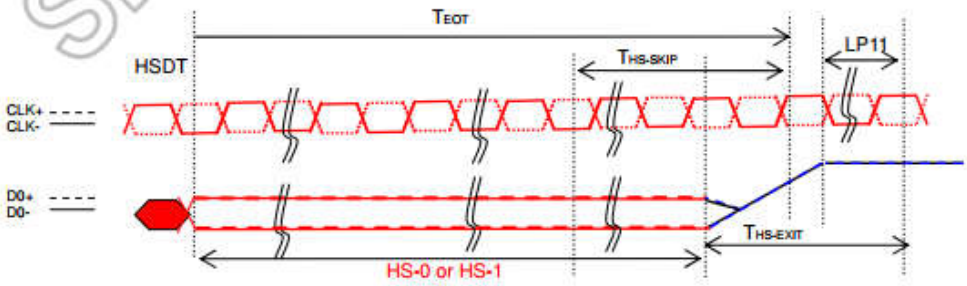
Table 7.4: DSI Low Power Mode Characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

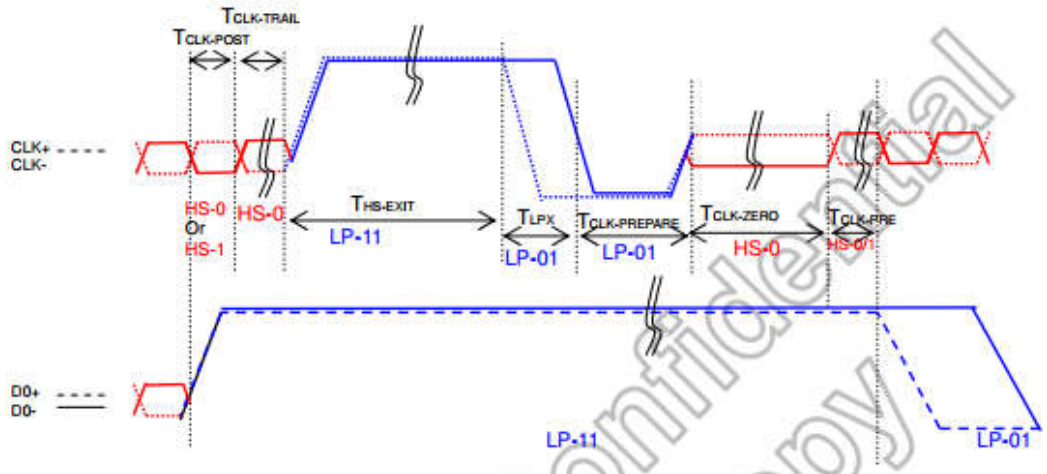
Table 7.5: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table 7.6: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

7.3.3 Reset input timing

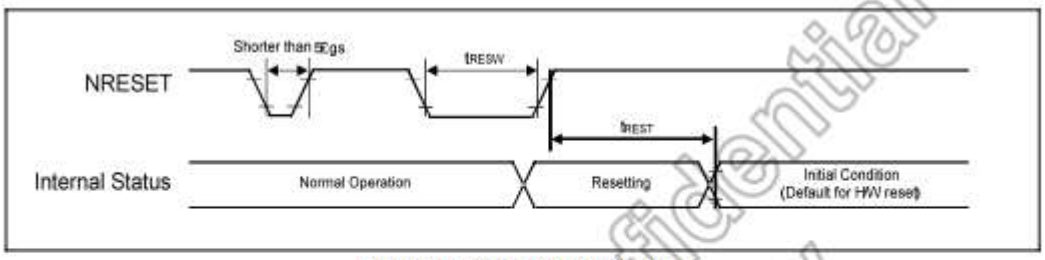


Figure 7.8: Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7.8: Reset Input Timing

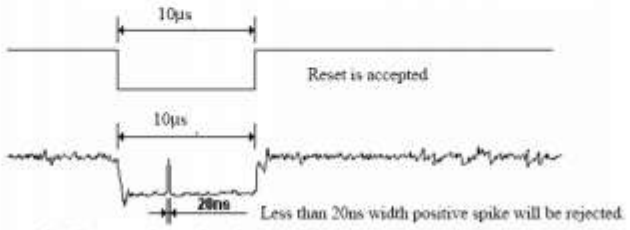
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

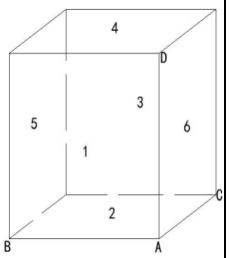
(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

5.可靠性实验测试(Reliability Test Conditions And Methods)

<table>
<tr><th>序号</th><th>试验项目</th><th>试验条件及方法</th><th>试验设备</th><th>检验项目</th><th>检验工具</th></tr>
<tr><td>1</td><td>高温高湿(静、动态)试验</td><td>温度 60℃±3℃,湿度 90%±3%,要求选择时间分别为 96 小时,静、动态（产品点亮）在室温下恢复 2 小时后进行外观,显示功能检查。</td><td>恒温恒湿试验机</td><td>检验外观、功能、抗腐蚀性</td><td rowspan="2">目视/测试架/客户样机/显微镜</td></tr>
<tr><td>2</td><td>高、低温冲击试验</td><td>静态-30℃（30 分钟）∽ 80℃（30 分钟）∽ -30℃（30 分钟），24 个循环，在室温下恢复 2 小时后进行外观,显示功能检查。</td><td>冷热冲击试验机</td><td>检验外观、功能</td></tr>
<tr><td>3</td><td>高温存贮试验</td><td>常温70℃+-3℃、宽温80℃+/-3℃、96小时后在室温状态下恢复1 小时在2 小时内完成外观、显示功能检查。</td><td>烤箱</td><td>检验外观、功能</td><td rowspan="2">目视/测试架/客户样机</td></tr>
<tr><td>4</td><td>低温存贮试验</td><td>常温-20℃+/-3℃、宽温-30℃+/-3℃、条件的试验箱内保存96小时后在室温状态下恢复1 小时,在2 小时完成外观、显示功能检查，特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。</td><td>低温冰箱</td><td>检验外观、功能</td></tr>
<tr><td>5</td><td>低温存贮试验（动态）</td><td>常温-20℃+/-3℃、宽温-30℃+/-3℃条件的试验箱内点亮刷屏，过程中每1小时观察一次，检查显示功能，如：异常，卡机，花屏等。特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。</td><td>低温冰箱</td><td>检验外观、功能</td><td>目视/测试架/客户样机</td></tr>
<tr><td>6</td><td>包装模组跌落试验</td><td>1、跌落重量及自由落体高度:（图二）
 

2、自由落体角度如下：
<table><tr><th>总重量</th><th>自由落体高度</th></tr><tr><td>0-9kg</td><td>92cm</td></tr><tr><td>9-25kg</td><td>76cm</td></tr><tr><td>25-45kg</td><td>53cm</td></tr><tr><td>45-68kg</td><td>46cm</td></tr><tr><td>大于 68kg</td><td>41cm</td></tr><tr><td></td><td></td></tr></table>1） 一角：A角
2） 三菱：A-B,A-D,A-C
3） 六面：面 1，面 2，面 3，面 4，面 5，面 6;</td><td>包装模组跌落架</td><td>测试电性能无异常、外观检验无破损，无脱离现象</td><td>目视/测试架/客户样机</td></tr>
</table>

7	盐雾试验	标准条件:中性盐雾试验（NSS 试验）：5%的氯化钠盐水溶液,溶液 PH 值中性（6.5～7.2），试验温度 35±2℃,盐雾的沉降率在 1～2ml/80cm².h 之间,时间 24h。2.其它特殊要求条件:醋酸盐雾试验(ASS 试验)：5%氯化钠溶液中配入冰醋酸,溶液 PH 值为 3 左右，试验温度 35±2℃,盐雾的沉降率在 1～2ml/80cm².h 之间，时间 24h。	盐雾试验设备	检验外观、功能，盐雾试验结果的判定方法，腐蚀物出现判定法：定性判定，试验后功能测试应 OK，外观观察产品无腐蚀现象产生。	目视/测试架/客户样机/显微镜
8	ESD 抗静电试验	测试架测试状态下试验：接触 4KV,非接触(空气) 8KV 放电测试	抗静电枪（尖头接触放电，圆头空气放电）	检验外观、功能	目视/测试架

6. 光电参数（Optical Characteristics）

3.0 OPTICAL SPECIFICATIONS

3.1 Overview

The test of Optical specifications shall be measured in a dark room(ambient luminance≤ 1 lux and temperature = 25±2℃) with the equipment of Luminance meter system (Topcon SR-UL1R and Westar TRD-100A) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°.The center of the measuring spot on the Display surface shall stay fixed.

The backlight should be operating for 30 minutes prior to measurement.

Measurement condition:

1. Backlight：1 BEF(0°) LED：硅酸盐 LED
2. Pol：SLP_ADS 消费类_No APF Up+HC/ Down+Clear

3.2 Optical Specifications

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle	Horizontal	Θ3	CR>10	80	85		°	Note 1
		Θ9		80	85		°	
	Vertical	Θ12		80	85		°	
		Θ6		80	85		°	
Contrast Ratio		CR	Θ= 0°	800	1000			Note 2
Transmittance		T(%)	Θ= 0°	2.7	3.2			Note 3
NTSC		%	Θ= 0°	65	69			
Reproduction Of color	Red	Rx	Θ= 0°	0.640	0.655	0.670		Note 4 *Color filter Glass W OC
		Ry		0.312	0.327	0.342		
	Green	Gx		0.269	0.284	0.299		
		Gy		0.579	0.594	0.609		
	Blue	Bx		0.123	0.138	0.153		
		By		0.096	0.111	0.126		
White		Wx	Θ= 0°	0.285	0.300	0.315		
		Wy		0.311	0.326	0.341		
Response Time		Tr+Tf	Θ= 0°		30	35	ms	Note 5

Note:

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIG.1).
2. Contrast measurements shall be made at viewing angle of Θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIG. 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the value without APF Pol.

4. The color chromaticity coordinates specified in Table1 shall be calculated from
The spectral data measured with all pixels first in red, green, blue and white.
Measurements shall be made at the center of the C/F.
Measurement condition is C - light source & Halogen Lamp
5. The electro-optical response time measurements shall be made as FIG.2 by switching the "data" input signal ON and OFF.
The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

Figure 1. Measurement Set Up

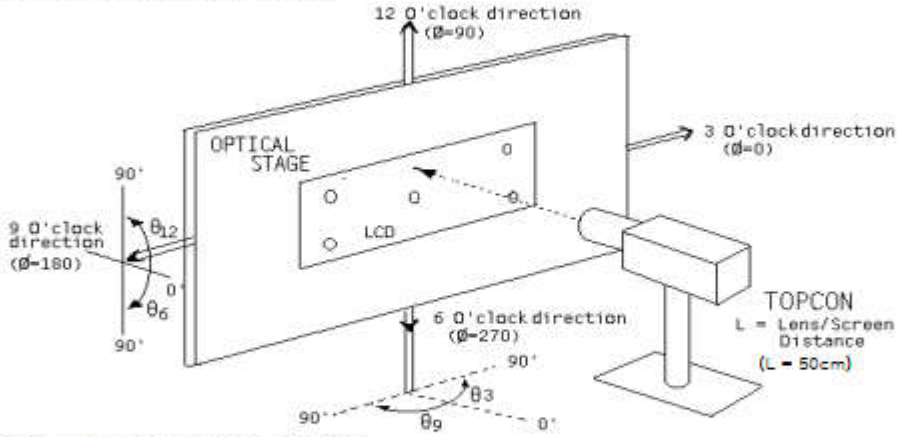
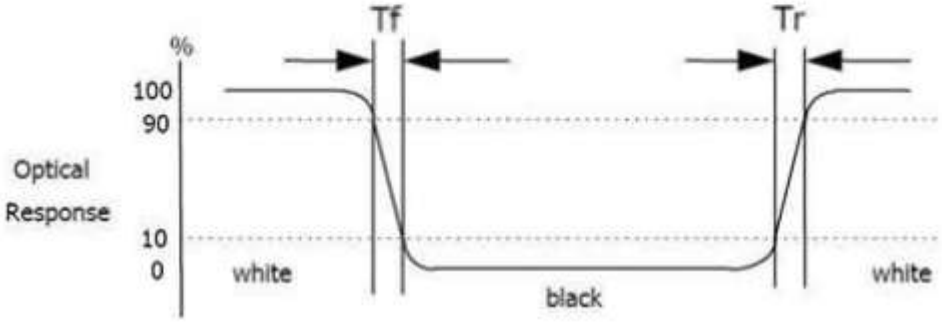
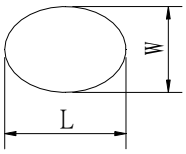
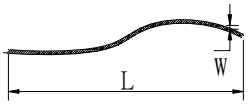
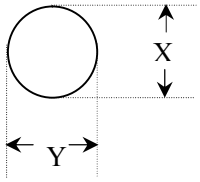


Figure 2. Response Time Testing



7.检验标准 (Inspection standard)

<table>
<tr><td>项目</td><td>不良定义</td><td>不良现象</td><td colspan="3">判定标准</td><td>检验方法</td><td></td></tr>
<tr><td>9.3.1</td><td>外观尺寸</td><td>与图纸尺寸不相符</td><td colspan="3">NG</td><td>卡尺</td><td></td></tr>
<tr><td rowspan="4">9.3.2</td><td rowspan="4">功能</td><td>显示少线</td><td colspan="3">NG</td><td>目视</td><td></td></tr>
<tr><td>无显示</td><td colspan="3">NG</td><td>目视</td><td></td></tr>
<tr><td>显示异常</td><td colspan="3">NG</td><td>目视</td><td>主</td></tr>
<tr><td>TP 功能不良，无触摸</td><td colspan="3">NG</td><td>目视/用手触摸</td><td>主</td></tr>
<tr><td>9.3.3</td><td>点亮产品可见及在 LCD 或 T/P 上有擦拭不掉的点状物</td><td>偏光片刺伤、脏点、圆形物、黑点
 

Φ=(L+W)/2</td><td colspan="3">LCM/总成＞2.4 寸——6.0 寸
Φ≦0.10mm：1、10mm 间距内只允许 3 个；2、显示区只允许 10 个点，超过以上任意一项则 NG
0.1mm＜Φ≦0.15mm：4（TP、屏各允许 2 个）
0.15mm＜Φ≦0.2mm：2（TP、屏各允许 1 个）
Φ＞0.2mm：NG</td><td>目 视(用菲淋卡比对)</td><td>次</td></tr>
<tr><td>9.3.4</td><td>点亮产品可见及在 LCD 或 T/P 上有擦拭不掉的线状物/刮伤</td><td> 
</td><td colspan="3">LCM/总成 0.95 寸——6.0 寸
长(L)≦1mm，宽(W)≦0.03mm：允许个数 2
长(L)≦2mm，0.03＜W≦0.05mm：允许个数 1
长(L)＞2mm，宽(W)＞0.05mm：NG
两条线毛之间必须距离 5mm 以上（0.95 寸—3.0 寸）.
两条线毛之间必须距离 10mm 以上（3.1 寸—6.0 寸）.</td><td>目视(用菲淋卡比对)</td><td>次</td></tr>
<tr><td>9.3.5</td><td>偏光片气泡</td><td>Φ=（X+Y）/2
 
</td><td colspan="3">尺寸：允许个数
1、Φ≦0.1mm；2、不超过边框 1/3：不计(密集不可)
0.10＜Φ≦0.2mm：1</td><td>在日光台灯下撕起保护膜，距待测物 30cm 目视</td><td>次</td></tr>
</table>

			Φ＞0.2mm	NG		
			0.95 寸-2.4 寸气泡间距大于 5mm 以上 ＞2.4 寸-6.0 寸气泡间距大于 10mm 以上			
9.3.6	T/P 及偏光片凹凸点	T/P:LCD 偏光片上有凹凸点	可视区有水纹（擦拭不掉）拒收 未进入可视区允收，客户装机后不见允收		在同一视角下用样品比对	次
9.3.7	Mura	边框四周或任一侧的色差、较画面深、区域云状不均、固定位置之图形凹陷状、封口部分较画面深的半圆形、一圈圈均匀的色差、线状 mura、黑画面可见因 spacer 聚集产生的 mura、均匀的实斜线、区域性斜线、Driver IC 与 TFT 匹配问题等原因的 mura	1.判定示画面为 128 灰阶画面，用 ND filter 盖住 mura 位置进行判定。 2、ND1.3（ND5%可遮盖不见） 3、双方若有签 限度样品，优先限度样品。		ND filter, 128 灰阶画面	次